Amendments to the Specification

Please amend the following paragraphs with the replacement paragraphs as marked up to show changes made. Each of these minor amendments are made to correct typographical errors.

[0024] The memory interface 250 and the bus 106 provide one or more media for transferring information to and from the memory module 210. Each bus component 220, 224, 226, 228 ordinarily transfers a selected type of information, i.e., address selection information on the address bus 224, data on the data bus 220, and command signals on the main control bus 226 and the supplementary control bus 228. Further, each bus may be suitably configured to transfer the relevant information. For example, each bus may be configured to handle a selected number of bits.

[0027] Command signals may be divided between the main control bus 226 and the supplementary control bus 228 in any suitable manner; similarly, the main control bus 226 and the supplementary control bus 228 may be configured in any suitable manner to accommodate the command signals. For example, in one embodiment illustrated in Figure 3, the main control bus 226 comprises a main command bus 410 having three main command bits (M-CMD), a main chip select bus bit 412 having one bit (M-CS), and a main bank selection bus 414 having two bits (M-BA). The three main command bits are suitably designated as a row address strobe (RAS), a column address strobe (CAS), and a write enable (WE). In the present embodiment, the main bank selection bus ~~222~~414 comprises a two-bit bus

which defines the bank to which a command is to be applied, and the one-bit main chip select bus 412 identifies the relevant chip for the corresponding operation.

[0030] Thus, the ACTIVE and subsequent READ or WRITE commands may be asserted using the main control bus 226 in conjunction with the address bus 224 to retrieve or store data. The next ACTIVE command or other command may then be asserted via the main control bus 226 on another bank ~~310B~~ 210B concurrently with assertion of a PRECHARGE command on the original bank ~~310A~~ 210A via the supplementary control bus 228. Accordingly, the PRECHARGE commands may be asserted without using the main control bus 226, thus relieving congestion on the main control bus 226 and tending to improve the performance of the memory module 210.

[0037] Further, referring to Figure 8, the secondary command ~~622~~ 722 may indicate another command following, such as in the next cycle, by asserting a tertiary command indicator 724 (EXTEND2). The tertiary command ~~726~~ 724 may then be asserted in the following cycle. Additional command capability may be provided using additional sub-command indicators if desired. Thus, many low priority commands may be added without adding additional command bits.